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Phase Shifted Carrier Pulse Width Modulation for Three Phase Multilevel Inverter to Minimize THD and Enhance Output Voltage Performance

This paper presents, a phase shifted carrier pulse width modulation is proposed, which can minimize the output total harmonic distortion and enhances the output voltages from five level inverter to multilevel topologies. Multilevel inverters are important for power electronics applications such as flexible ac transmission systems, renewable energy sources, uninterruptible power supplies and active power filters. Two novel methodologies adopting the phase shifted carrier pulse width modulation concept are proposed in this paper. The phase shifted carrier pulse width modulation cascaded multilevel inverter strategy minimized output total harmonic distortion and phase shifted carrier switching frequency optimal pulse width modulation cascaded multilevel inverters strategy enhances the output voltages. Field programmable gate array has been chosen to implement the pulse width modulation due its fast proto typing, simple hardware and software design. Simulation and Experimental results are provided.

Keywords: Phase shifted pulse width modulation, Switching frequency optimal pulse width modulation, Total harmonic distortion, Output voltage, Cascaded Multilevel inverter.

1. Nomenclature

FPGA Field programmable gate array.
m Number of output phase voltage levels in a cascaded inverter.
s Number of separate dc sources.
PSC PWM Phase shifted carrier pulse width modulation. n_p Number of pole pairs.
PSC-SFO PWM Phase shifted carrier switching frequency optimal pulse width modulation.
L Number of switched DC levels.
V_{oi} Output voltage of cell i.

2. Introduction

Recently, for increasing use in practice and fast developing of high power devices and related control techniques, multilevel inverters have become more attractive to researches and industrial companies [1]. Multilevel inverters have achieved an increasing contribution in high performance applications [2]-[5]. This paper, the name phase shifted carrier pulse width modulation is used for proposed inverter control methods. Since, they are all based on the phase shifted carrier concept. The control objective is to compare reference and phase shifted carrier wave using three phase five level cascaded inverter[6],[8]. The multilevel inverter advantages are improved output voltage, reduced output total harmonic distortion, reduced voltage stress on semiconductors switches and decreases of EMI problems[6],[9].

The different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitors multilevel inverters. Increasing the number of levels in the inverter without requiring high ratings on individual devices can increases the power rating [10]. In this paper, two novel phase shifted carrier pulse width modulation schemes are present

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[11]-[13] which take advantage of special properties available in multilevel inverter to minimize total harmonic distortion and increases output voltage [14]. Illustrative examples are given to demonstrate the feasibility of the proposed methods.

3. Three Phase Cascaded Multilevel Inverter

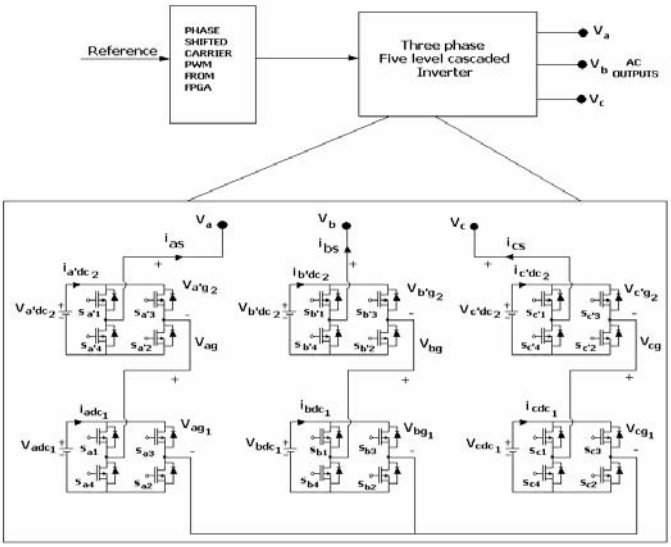

Fig. 1: FPGA based three phase cascaded five level inverter

A Field programmable gate array based three phase structure of five level cascaded inverter is illustrated in fig.1. Each dc source is connected to a three phase inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches. The ac outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascaded inverter is defined by m=2s+1, where s is the number of separate dc sources.

4. Phase Shifted Carrier Pulse Width Modulation (PSC PWM)

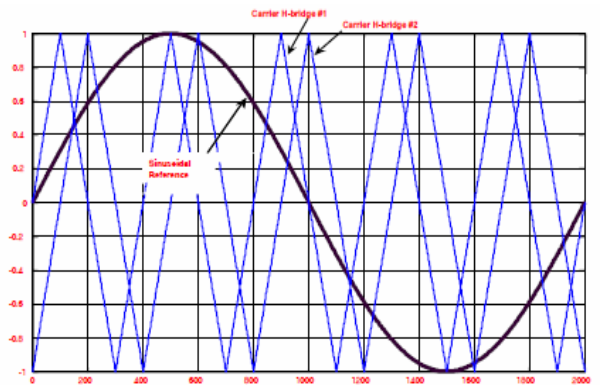

Fig. 2: Phase shifted carrier pulse width modulation

Fig.2 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180°/m for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

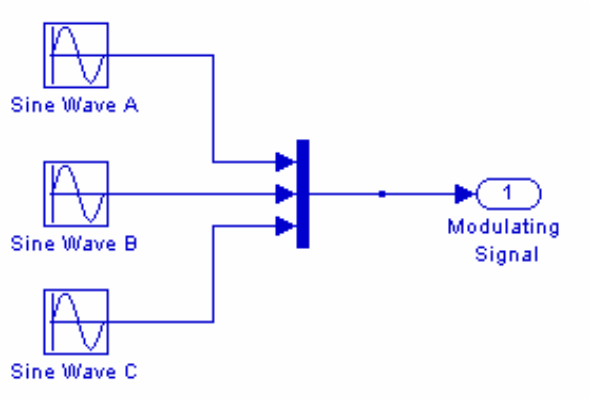

Fig. 3: PSC PWM Modulating signal generation

Fig.3 shows the phase shifted carrier pulse width modulation modulating signal generation. Optimum harmonic cancellation is achieved, Phase shifting each Carrier by,

$$(K-1)\Pi/n \quad (1)$$

Where, k is the kth inverter.

n is the number of series connected single phase inverter.

$$n= (L-1)/2 \quad (2)$$

Where, L is the number of switched DC levels that can be achieved in each phase Leg.

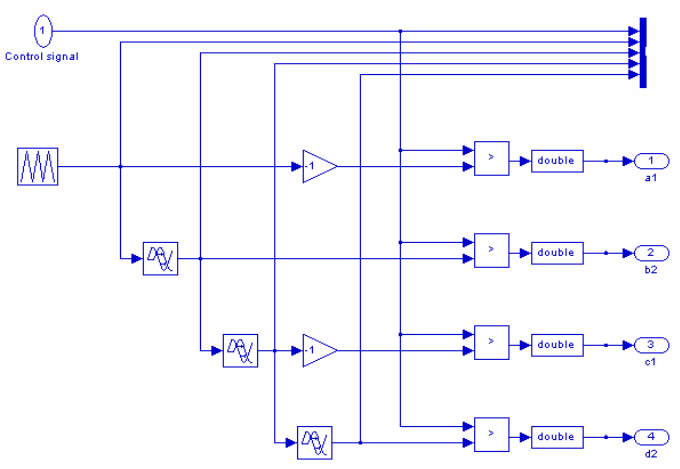

Fig. 4: PSC PWM signal generation

Fig.4 shows the phase shifted carrier pulse width modulation. The phase shifted carrier pulse width modulation for a particular power cell i of a cascaded multilevel inverter, with V_{dc} is constant. The average output voltage over one carrier cycle T_{cr} is

$$V_{oi} = 1/ T_{cr} \ . \int V_{oi}(t)dt \quad (3)$$

$$V_{oi} = T_{on}/T_{cr} \ . \ V_{dc} \quad (4)$$

$$V_{oi} = V \quad (5)$$

Where, V_{oi} is the output voltage of cell i, and T_{on} is the time interval, determined by the comparison between the reference and the carrier signals, in which the inverter generates the high level.

5. Phase Shifted Carrier Switching Frequency Optimal Pulse Width Modulation (PSC-SFO PWM)

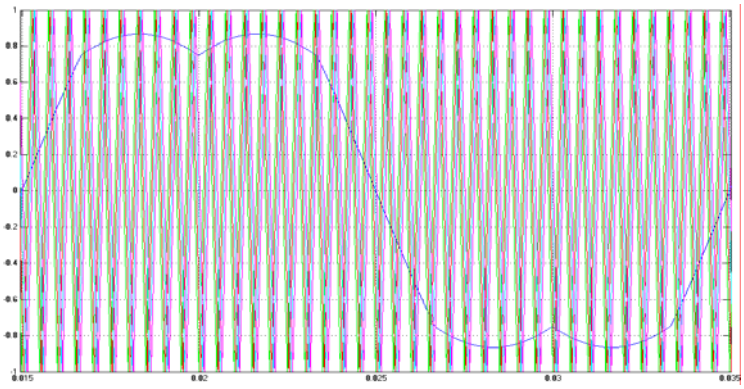

Fig. 5: Phase shifted carrier switching frequency optimal pulse width modulation

Fig.5 shows the phase shifted carrier switching frequency optimal pulse width modulation. Fig.6 shows the phase shifted carrier SFO PWM modulating signal generation. The method takes the instantaneous average of the maximum and minimum of the three reference voltages (V_a, V_b, V_c) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms.

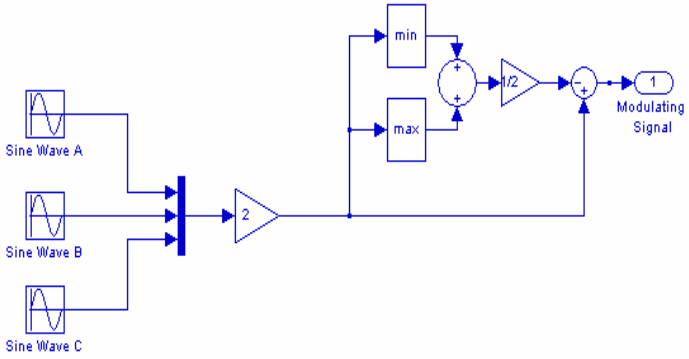

Fig.6: PSC-SFO PWM modulating signal generation

$$V_{offset} = \{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)\} / 2 \quad (6)$$

$$V_aSFO = V_a - V_{offset} \quad (7)$$

$$V_bSFO = V_b - V_{offset} \quad (8)$$

$$V_cSFO = V_c - V_{offset} \quad (9)$$

The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs.

5. Results

The table.1 shows THD and output voltage value for PSC PWM and PSC-SFO PWM. When modulation Index is more than 1, it is called as over modulation and if it's below or equal to 0.5 than it is called low modulation Indices.

TABLE 1
OUTPUT VOLTAGE AND THD FOR PSC PWM AND PSC-SFO PWM

Modulation Index	PSC PWM		PSC-SFO PWM	
	THD%	V_{ac}	THD%	V_{ac}
1.1 (Over Modulation)	3.84	10.65	21.03	11.86
1.0	0.75	10.15	20.92	11.43
0.9	0.35	10.01	20.65	11.01
0.8	1.05	09.36	20.51	10.04
0.7	2.45	08.58	20.72	09.32
0.6	4.60	06.32	21.02	07.82
0.5 (Low Modulation)	6.83	5.039	21.24	5.047

A. Simulation results

To verify the proposed schemes, a simulation model for a three phase five level cascaded H-Bridge inverter is implemented. The simulation parameters are as following 5KW rating, three phase load R = 100 ohms, L = 20mH, each source V_{dc} = 5V, switching frequency 5KHz. Diagrams of the phase leg voltages have been calculated and drawn for PSC PWM Method in Fig.7, 8.

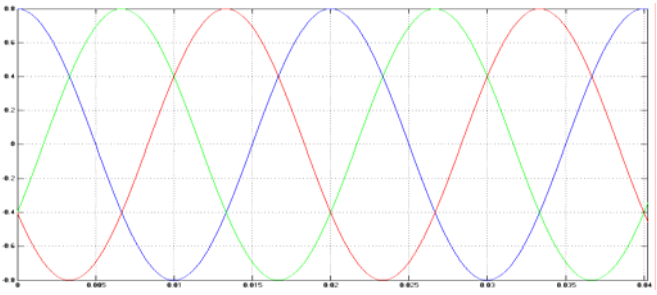

Fig.7: PSC PWM modulating signal

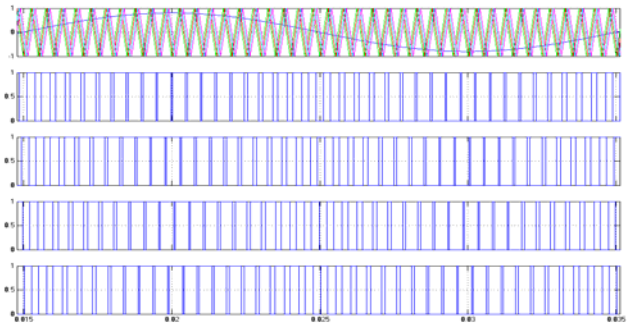

Fig.8: PSC PWM signal generation

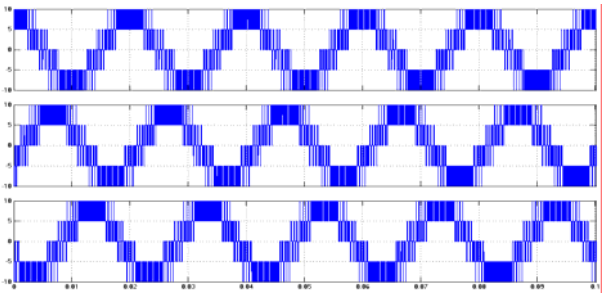

Fig.9: PSC PWM output voltage (Modulation index 0.9)

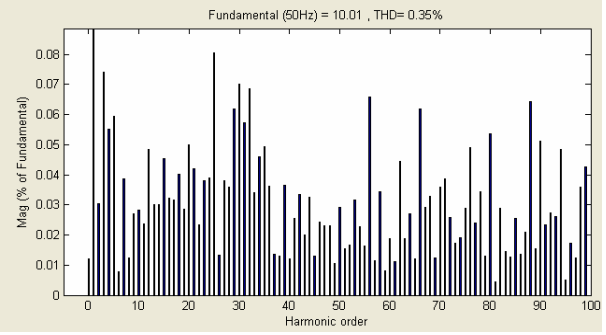

Fig.10: PSC PWM Harmonic spectrum (Modulation index 0.9)

Fig.9 and Fig.10 shows the output voltage of PSC PWM with modulation index 0.9, fundamental frequency 50Hz and THD value is 0.35% with output voltage of 10.01V. Fig.11 shows the output voltage and harmonic spectrum with modulation index 1.1. The THD value is 3.84% with output voltage of 10.65V. Fig.12 shows the output voltage and harmonic spectrum with modulation index 0.5. The THD value is 6.83% with output voltage of 5.039V.

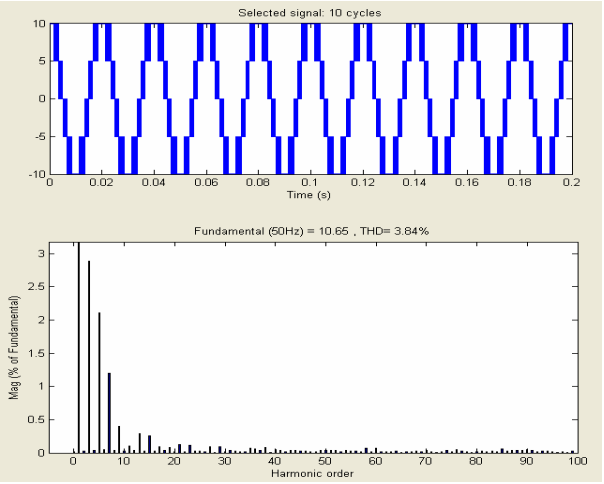

Fig.11: PSC PWM output voltage and harmonic spectrum (Modulation index 1.1)

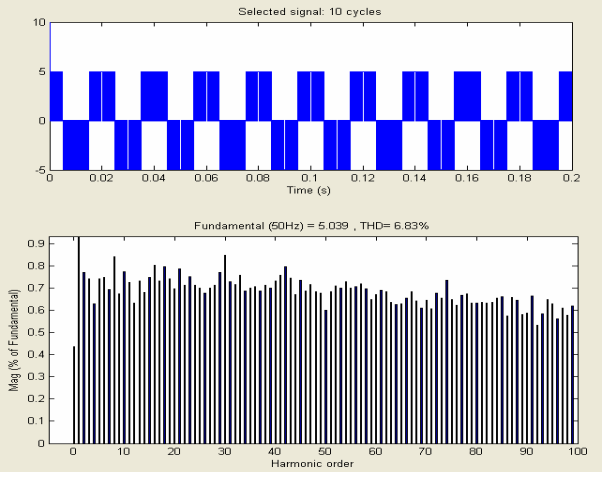

Fig.12: PSC PWM output voltage and harmonic spectrum (Modulation index 0.5)

Diagrams of the phase leg voltages have been calculated and drawn for PSC-SFO PWM method in Fig.13, 14.

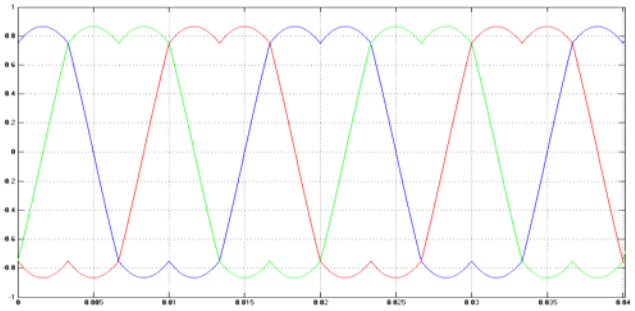

Fig.13: PSC-SFO PWM Modulating signal

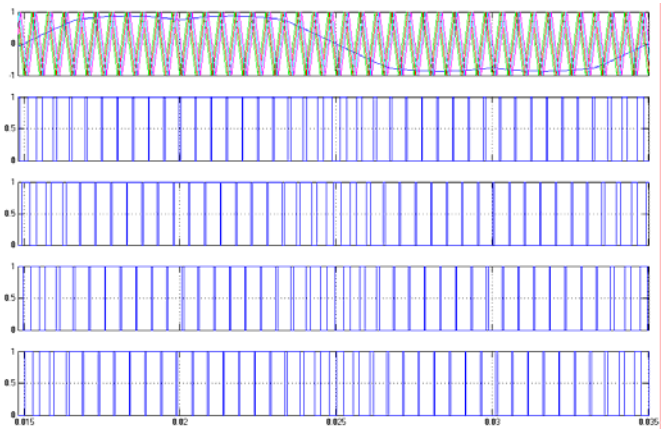

Fig.14: PSC-SFO PWM signal generation

Fig.15 and Fig.16 shows the output voltage of PSC-SFO PWM with modulation index 0.9, fundamental frequency 50Hz and THD value is 20.65% with output voltage of 11.01V. Fig.17 shows the output voltage and harmonic spectrum with modulation index 1.1. The THD value is 21.03% with output voltage of 11.86V. Fig.18 shows the output voltage and harmonic spectrum with modulation index 0.5. The THD value is 21.24% with output voltage of 5.047V.

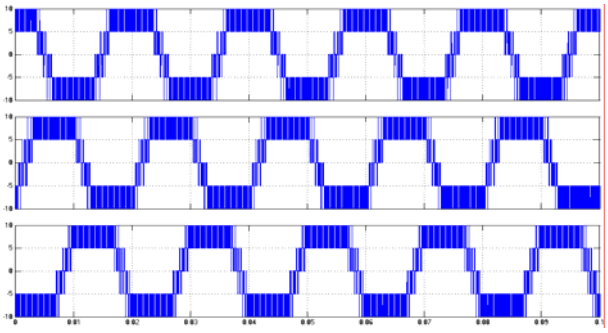

Fig.15: PSC-SFO PWM output voltage

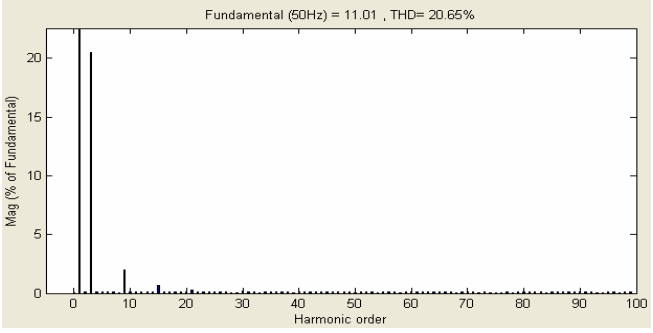

Fig.16: PSC-SFO PWM Harmonic spectrum

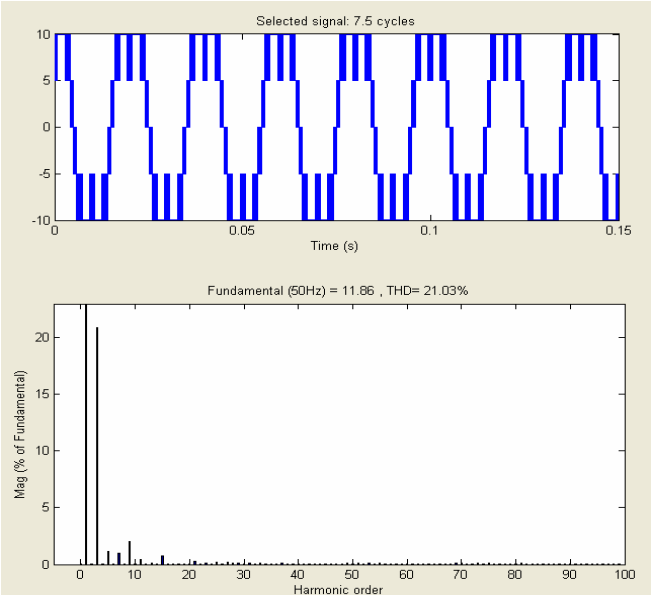

Fig.17: PSC-SFO PWM output voltage and harmonic spectrum (Modulation index 1.1)

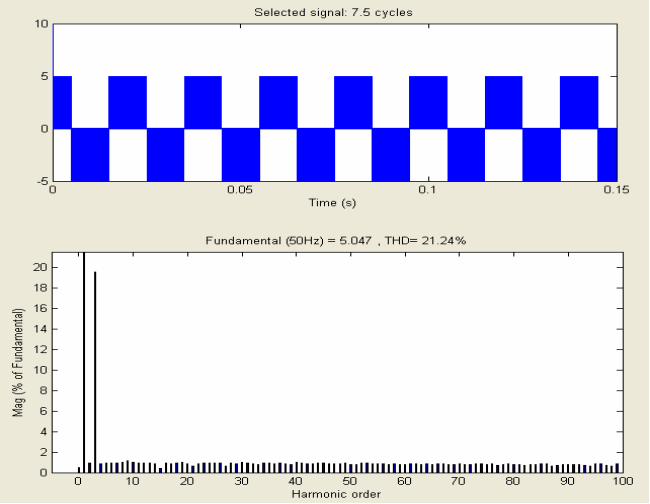

Fig.18: PSC-SFO PWM output voltage and harmonic spectrum (Modulation index 0.5)

B. Hardware Results

A hardware setup of three phase five level cascaded inverter has been built to validate the theoretical analysis. The hardware parameters are as following, 5KW rating, three phase load R = 100 ohms, L = 20mH, each source V_{dc} = 5V, fundamental frequency 50HZ, switching frequency 5KHZ and Xilinix Spartan – DSP controller (FPGA). The three phase output voltage waveform for PSC PWM method shown in fig.19, 20, 21 and PSC-SFO PWM method shown in fig.22, 23, 24.

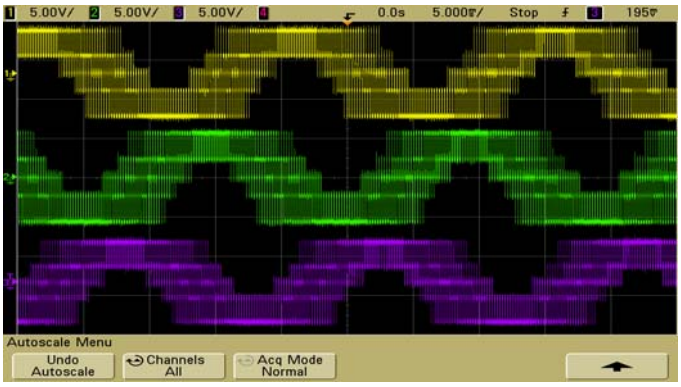

Fig.19: PSC PWM output voltage

Fig.20: PSC PWM output voltage
(Modulation index 1.1)

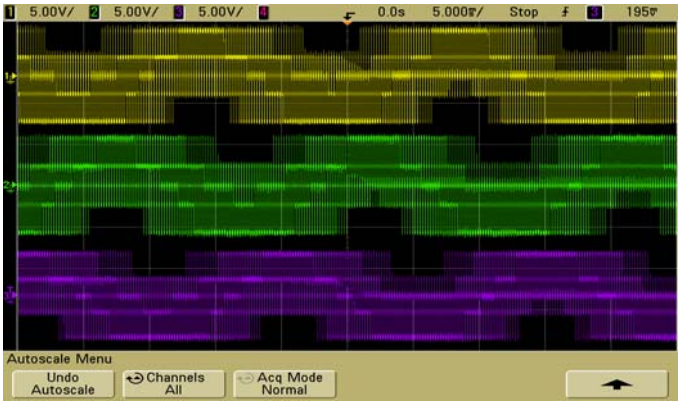

Fig.21: PSC PWM output voltage
(Modulation index 0.5)

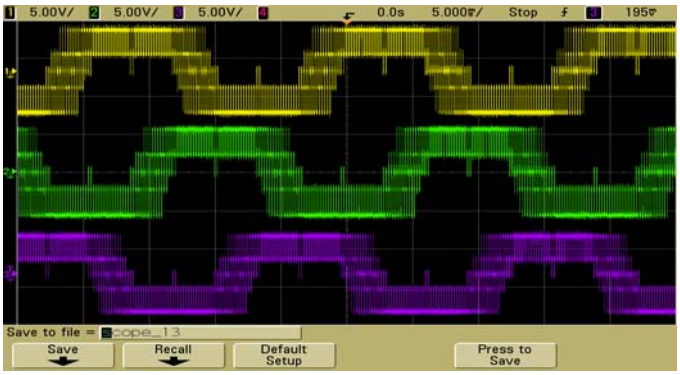

Fig.22: PSC-SFO PWM output voltage

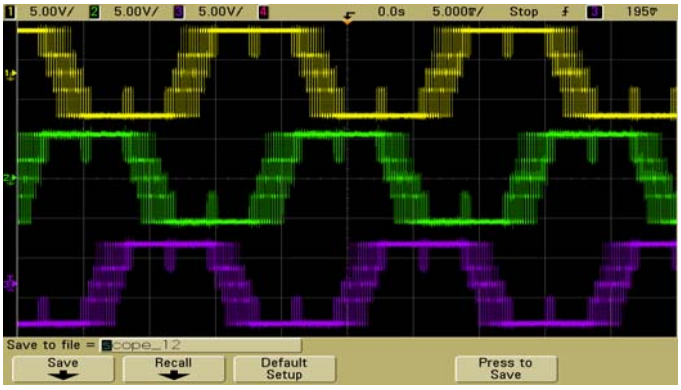

Fig.23: PSC-SFO PWM output voltage
(Modulation index 1.1)

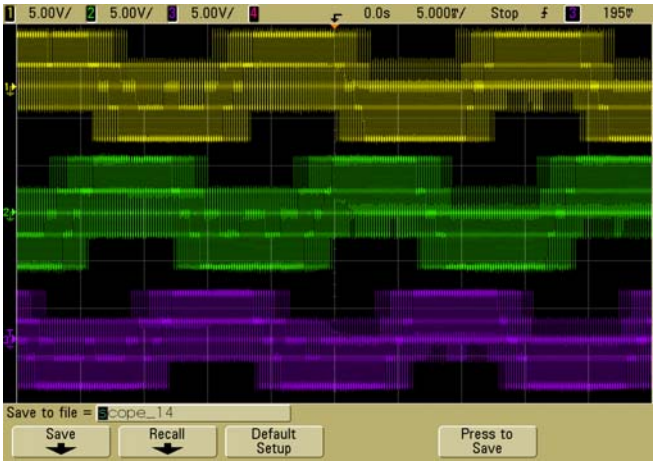

Fig.24: PSC-SFO PWM output voltage
(Modulation index 0.5)

Fig.25: Hardware setup of three phase cascaded multilevel inverter

5. Results

In this paper, two new schemes adopting the phase shifted pulse width modulation concept are proposed. The PSC PWM strategy reduces the THD and PSC-SFO PWM strategies enhances the fundamental output voltage. The multilevel inverter improves output voltage, reduces output total harmonic distortion and voltage stress on semiconductors switches. By adopting PSC PWM strategy with modulation index equal to 0.9, the THD value is reduced to 0.35 and output voltage is obtained to 10.01V. To increase the output voltage value to 11.01V, PSC-SFO PWM strategy is used. Those schemes confirmed by simulation results and experimental results.

References

[1] K.A Corzine, and Y.L Familiant, "A New Cascaded Multi-level H-Bridge Drive," IEEE Trans. Power.Electron., vol.17, no.1, pp.125-131. Jan 2002.

[2] J.S.Lai, and F.Z.Peng "Multilevel converters – A new bread of converters,"IEEE Trans. Ind.Appli., vol.32, no.3, pp.509-517. May/Jun.1996.

[3] T.A.Maynard, M.Fadel and N.Aouda, "Modelling of multilevel converter," IEEE Trans. Ind.Electron., vol.44, pp.356-364. Jun.1997.

[4] P.Bhagwat, and V.R.Stefanovic, "Generallized structure of a multilevel PWM Inverter," IEEE Trans. Ind. Appln.., vol.1A-19, no.6, pp.1057-1069. Nov./Dec..1983.

[5] J.Rodriguez, Jih-sheng Lai, and F Zheng peng, "Multilevel Inverters; A Survey of Topologies, Controls, and Applications," IEEE Trans.Ind.Electron., vol.49 , no4., pp.724-738. Aug.2002.

[6] G.Carrara, S.Gardella, M.Marchesoni, R.salutari,and G.sciutto, "A New Multilevel PWM Method; A theoretical analysis," IEEE Trans. Power.Electron., vol.7, no.3, pp.497-505. Jul.1992.

[7] L.M.Tolber, T.G.Habetler, "Novel Multilevel Inverter Carrier based PWM Method," IEEE Ind.Appli., vol.35. pp.1098-1107. Sep/Oct 1999.

[8] Roozbeh Naderi, and Abdolreza rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," IEEE Trans. Power.Electron., vol.23, no.3, pp.1257-1269. May.2008.

[9] Samir koaro, PabloLezana, Mauricio Anguio, and Jose Rodriguez, "Multicarrier PWM DC-Link ripple forward compensation for multilevel inverters," IEEE Trans. Power.Electron., vol.23, no.1, pp.52-56. Jan 2008.

[10] P.Palanivel and Subhransu Sekhar Dash, "Multi carrier pulse width modulation based three phase cascaded multilevel inverter including over modulation and low modulation indices," RI Pub. Int. Journ. Eng. Studies. Vol.1, no.2, pp.71-82. June 2009.

[11] P.Palanivel and Subhransu Sekhar Dash, "A FPGA based variable switching frequency multicarrier pulse width modulation for three phase cascaded multilevel inverter," Proc. IEEE INCACEC-2009. Kongu Engineering college, Erode, India, pp.1-4. June 2009.
[12] P.Palanivel, and Subhransu Sekhar Dash, "Analysis and implementation of multicarrier pulse width modulation based three phase cascaded multilevel inverter," UPA Int. Journ. Power sys. and Power Electron. Vol2, no.1, pp.70-75. June 2009.
[13] P.Palanivel, and Subhransu Sekhar Dash, "Comparative study of constant switching frequency and variable switching frequency multicarrier pulse width modulation for three phase multilevel inverter," Aca. Pub. Int. Journ. recent trends in Eng. Vol.2, no.1, pp.49-52. June 2009.
[14] B.P.McGrath, Holmes , and T.Meynard, "Reduced PWM Harmonic distortion for multilevel inverter operating over a wide modulation range, " IEEE Trans. Power.Electron., vol.21, no.4, pp.941-949. Jul.2006.